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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,537	12/18/2001	Ivo Wilhelmus Johaooes Marie Rutten	US 018205	2844

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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 09/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,537	RUTTEN, IVO WILHELMUS JOHAOOES MARIE	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *24 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 5-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 5-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Pending claims 1, 3, and 5-18 have been examined. Claims 1, 5, 11, 15, 17, and 18 have been amended.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 3, and 5-18 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claim 3 is objected to because of the following informalities: This claim is still depending on cancelled claim 2. For purpose of examination the Examiner with read this claim as depending on claim 1. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 18:

This claim recites the limitation "the other devices-under -test" in lines 4-7. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1,3, 5, 6, 8-17 rejected under 35 U.S.C. 102(e) as being anticipated by Tsujii (US-6489791), hereinafter Tsujii.

Claim 1, 11 and 17:

Tsujii teaches BOST LSI 1008 (Build Off Self Test) (programmable integrated circuit) receives a simple control signal (configured to receive the test command) from a tester 1001 (a computer) and then generates test signals necessary for testing a device-under-test 1007 (DUT), checks to see if output signals from the DUT 1007 are correct, and notifies the tester 1001 of the results of the tests on the DUT 1007. (Col. 1, lines 32-37). Tsujii continues to teach a BOST LSI 8 (programmable integrated circuit) and a DUT 7 are mounted on a single socket 12 (programmable integrated circuit and DUT are vertically aligned and in immediate proximity of each other) which brings electrodes of the BOST LSI 8 and DUT 7 into direct contact with one another for testing

(programmable integrated circuit includes at least one point that is arranged to provide direct contact to the DUT). Tsujii also teaches signals of a tester 1 (ATE, a computer) are input to the BOST LSI 8 via POGO pins 2 of the tester 1 (coupled to the ATE), printed wiring 10 of a test board 3, and contactors 6 of the socket 12 (interface circuit). Tsujii further teaches the signals are exchanged at low speeds between the tester and the BOST LSI 8 and high-speed signals for testing the DUT 7 are fed from the electrodes of the BOST LSI 8 directly to the electrodes of the DUT 7. (Col. 2, lines 61-67, col. 3, lines 1-6).

Claim 3:

Tsujii teaches a BOST LSI 8 (programmable integrated circuit) and a DUT 7 are mounted on a single socket 12 (programmable integrated circuit and DUT are vertically aligned and in immediate proximity of each other) which brings electrodes (bond pad) of the BOST LSI 8 and DUT 7 into direct contact with one another for testing (programmable integrated circuit includes at least one point that is arranged to provide direct contact to the DUT). (Col. 2, lines 61-64).

Claim 5:

Tsujii teaches BOST LSI 1008 (Build Off Self Test) (programmable integrated circuit) receives a simple control signal (configured to condition the test command) from a tester 1001 (ATE, a computer) and then generates test signals necessary for testing a device-under-test 1007 (DUT), checks to see if output signals from the DUT 1007 are correct, and notifies the tester 1001 of the results of the tests on the DUT 1007 (ATE configured to receive test response). (Col. 1, lines 32-37).

Claim 6:

Tsujii teaches the BOST involves mounting on a test board an LSI or circuits for expediting examinations of a device under test (called the DUT hereunder, including an LSI or the like to be tested in bare-chip or packaged form). In this configuration a probe card would be need to test the bare-chip DUT and therefore is inherent. (Col. 1, lines 15-17).

Claim 8:

Tsujii teaches signals of a tester 1 (ATE, a computer) are input to the BOST LSI 8 via POGO pins 2 of the tester 1, printed wiring 10 of a test board 3, and contactors 6 of the socket 12 (interface circuit). Tsujii also teaches that the signals are exchanged at low speeds between the tester and the BOST LSI 8 (first bandwidth) and high-speed signals for testing the DUT 7 are fed from the electrodes of the BOST LSI 8 directly to the electrodes of the DUT 7 (second bandwidth). (Col. 2, lines 65-67, col. 3, lines 1-6).

Claim 9:

Tsujii teaches that the DUT is a semiconductor LSI circuit. (Col. 1, lines 15-17).

Claim 10:

Tsujii teaches BOST LSI 1008 (Build Off Self Test) (programmable integrated circuit) receives a simple control signal (the test command is a subroutine) from a tester 1001 (ATE, a computer) and then generates test signals necessary for testing a device-under-test 1007 (DUT) (configured to generate the at least on test signal), checks to see if output signals from the DUT 1007 are correct, and notifies the tester 1001 of the results of the tests on the DUT 1007 (Col. 1, lines 32-37).

Claims 12 and 13:

Tsujii teaches a BOST LSI 8 (programmable integrated circuit) and a DUT 7 are mounted on a single socket 12 which brings electrodes (plurality includes a bonding pad) of the BOST LSI 8 and DUT 7 into direct contact with one another for testing. (Col. 2, lines 61-64).

Claims 14, 15 and 16:

Tsujii teaches a BOST LSI 1008 (programmable integrated circuit) that receives a simple control signal from a tester 1001 then generates test signals necessary for testing a DUT 1007 (configured to condition the test signals, claim 14), checks to see if output signals from the DUT 1007 are correct (configured to receive a response signal from the DUT, claim 15), and notifies the tester 1001 of the results of the tests on the DUT 1007 (generate the at least one test response). (Col. 1, lines 32-37). Although Tsujii does not disclose the detail of the BOST LSI, it is well known in the art that BOST (Built-Off-Self-Test) devices typically comprise of such components as, but not limited to, a high frequency oscillator to facilitate DUT clock generation, an AD/DA converters, a controller, a DSP analyzer, a memory, a test pattern generator, and a comparator circuit (other components, claim 16).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsujii (US-6489791), hereinafter Tsujii, in view of Arkin et al. (US-6028439).

Claims 7 and 18:

Tsujii does not explicitly teach "programming other programmable integrated circuits" (a plurality) and "placing the other programmable integrated circuits in proximity to other devices-under-test" (a plurality). However, Tsujii does teach the BOST LSI 1008 and DUT 1007 are mounted on different sockets 1012 attached to a test board 1003 probe board) and exchange relevant signals through printed wiring 1010 (provide a direct communication). (Col. 1, lines 38-40). Arkin teaches a modular integrated circuit tester 10 (ATE) that performs a sequence of tests on one or more (other devices-under-test) integrated circuit devices under test (DUT) 12 which also includes a set of tester modules 14(1)-(3) (programmable integrated circuit), each of which conducts all test activities at a corresponding set of terminals of DUT 12 during each test and can be expanded to include a larger number of tester modules (other programmable integrated circuits). (Col. 4, lines 44-53). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tsujii's test board 1003 (probe card) accommodate Arkin's tester modules 14(1)-(3) (programmable integrated circuit). The artisan would have been motivated to do so because this would enable Tsujii's testing system to test a plurality of DUT's simultaneously.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133

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